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LETTER

A Neuro Fuzzy Solution in the Design of Analog Circuits

Pedro MIRANDA-ROMAGNOLI[†a)], ***Member***, **Norberto HERNÁNDEZ-ROMERO**[††], ***and*** **Juan C. SECK-TUOH-MORA**[††], ***Nonmembers***

SUMMARY A neuro fuzzy method to design analog circuits is explained, where the universe of discourse of the fuzzy system is adjusted by means of a self-organized artificial neural network. As an example of this approach, an op-amp is optimized in order to hold a predetermined aim; where the unity gain bandwidth is an objective of design, and the restrictions of open-loop gain and margin phase are treated as objectives too. Firstly, the experience of the behavior of the circuit is obtained, hence an inference system is constructed and a neural network is applied to achieve a faster convergence into a desired solution. This approach is characterized by having a simple implementation, a very natural understanding and a better performance than static methods of fuzzy optimization.

key words: *neuro fuzzy design, analog circuits, operational amplifier, optimization*

1. Introduction

The development of circuit-design tools has been a dynamic field since the early 1970s, due to the continuous increment in circuit complexity. The techniques proposed to reduce the time needed for the design process, are based on a large number of different techniques; some of them handling the matrix of the circuit, others dealing with this task as an optimization problem and solving it making use of traditional procedures, such as gradient or quasi-Newton methods. A survey of these optimization techniques is made in [1] and a review of tools for automation design can be found in [2]. In [3], [4] an approach employing an optimal control formulation for small circuits is presented.

Some examples of fuzzy logic tools are FPAD [5] and FASY [6]. In [7], a fuzzy method is presented for multi-objective optimization. The use of Adaptive Neuro Fuzzy Inference System (ANFIS) [8] for the design of CMOS gates was reported in [9], where it requires a very long, time consuming process for training the neurons involved in this type of implementation.

In this manuscript, unsupervised Kohonen-like neural networks [10] are applied to adjust the fuzzy universe of discourse, in order to improve an analog circuit design, in terms of time. We are making use of two networks, one attached to the input and the other associated to the output of the fuzzy system.

The remainder of the paper is organized as follows: Sect. 2 formulates the design issue as a fuzzy optimization problem, Sect. 3 explains the fuzzy system used for achieving the objectives and restrictions of the circuit design. Section 4 explains how the universe of discourse of the fuzzy systems are adjusted by means of the proposed Kohonen-like networks. Finally, Sect. 5 provides some comments about the benefits obtained with the suggested method.

2. Problem Formulation

A circuit design is determined by k independent parameters and m dependent ones (nodal voltages), which may be grouped into a single vector $\mathbf{x} = (x_1, \ldots x_k, x_{k+1}, \ldots, x_{k+m})$. In a similar way, the l design objectives can be arranged as follows:

$$\mathbf{f}(\mathbf{x}) = (f_1(\mathbf{x}), f_2(\mathbf{x}), \ldots, f_l(\mathbf{x})), \tag{1}$$

hence, the design can be expressed as an optimization problem:

$$\begin{array}{ll} \text{minimize} \ \| \mathbf{f}(\mathbf{x}) \| & \\ \quad \mathbf{x} \in \mathbb{R}[n] & \\ \text{Subject to:} & \\ g_p \geq spec_{g_p} & p = 1 \cdots r \\ spec_{h_{q\_min}} \leq h_q \leq spec_{h_{q\_max}} & q = 1 \cdots s \\ x_{min} \leq x_j \leq x_{max} & j = 1 \cdots k \end{array} \tag{2}$$

where $\mathbf{f} : \mathbb{R}[n] \rightarrow \mathbb{R}[l]$ with $n = k + m$; function $\mathbf{f}$ maps the input space into the output one. Each constraint g_p is satisfied when it is major or equal than a pth specification $spec_{g_p}$. Every constraint h_q is satisfied when it is between the qth specified limits h_{q_min} and h_{q_max}. Finally, x_{min} and x_{max} are the minimum and maximum permitted values for the independent parameters.

For a fuzzy optimization, the concept of satisfiability means that an objective design f_i has an associated membership function μ_{f_i}. Similarly, inequality constraints $g_p(\mathbf{x})$ and $h_q(\mathbf{x})$ have associated membership functions μ_{g_p} and μ_{h_q}. Let $\mu(\mathbf{x})$ describe the group of grades of membership, which is defined as follows:

$$\begin{aligned} \mu(\mathbf{x}) = (&\mu_{f_1}(\mathbf{x}), \mu_{f_2}(\mathbf{x}), \ldots, \mu_{f_l}(\mathbf{x}), \\ &\mu_{g_1}(\mathbf{x}), \mu_{g_2}(\mathbf{x}), \ldots, \mu_{g_r}(\mathbf{x}), \\ &\mu_{h_1}(\mathbf{x}), \mu_{h_2}(\mathbf{x}), \ldots, \mu_{h_s}(\mathbf{x})) \end{aligned} \tag{3}$$

every μ_{f_i}, μ_{g_p} and μ_{h_q} belong to the interval $[0, 1]$. Values

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[†]The author is with the Department of Mathematics and Physics, Autonomous University of Hidalgo, Mexico.
[††]The authors are with the Department of Industrial Engineering, Autonomous University of Hidalgo, Mexico.
a) E-mail: pmiranda@uaeh.edu.mx

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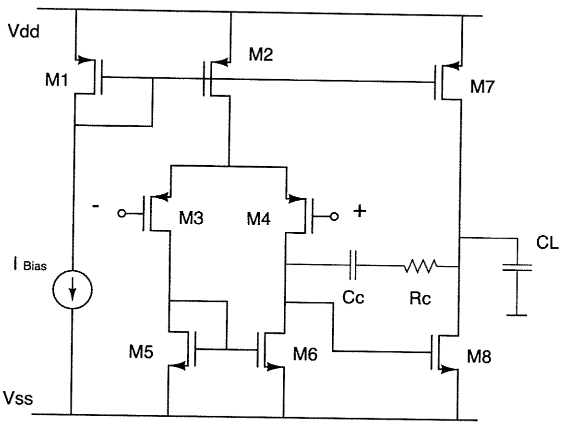


Fig. 1 Two-stage operational amplifier.

close to 1 indicate a greater grade of membership and consequently a major satisfiability; on the contrary values near to 0 represent a minor grade of membership. Therefore, the problem in Eq. (2) may be expressed as:

$$\begin{array}{l} \text{maximize } \parallel \mu(\mathbf{x}) \parallel \\ \mathbf{x} \in \mathbb{R}[n] \\ \text{Subject to:} \\ x_{min} \leq x_j \leq x_{max} \quad j = 1 \cdots k \end{array} \tag{4}$$

Figure 1 shows our case of study, a two-stage operational amplifier (op-amp) [11]. It has two amplifier stages with 13 parameters of design, 8 corresponding to the MOS transistors and 5 corresponding to the nodal voltages. Our main goal is to accomplish certain Unity Gain Bandwidth (UGB); thus a membership function μ_f has been assigned to UGB. Besides the size of transistors, other restrictions are: a minimum Open Loop Gain (OLG) and a Phase Margin (PM) within a region that allows the correct operation of the op-amp. Both restrictions are handled as design objectives through membership functions μ_g and μ_h, which are explained in next section.

The first amplification stage of the op-amp has the restriction that transistors M_3 and M_4 must be equal, therefore their widths W_3 and W_4, and their largenesses L_3 and L_4, must accomplish the next equality constraints:

$$W_3 = W_4,\ L_3 = L_4. \tag{5}$$

Similarly, transistors of current mirrors formed by M_1 and M_2, and M_5 and M_6 are equal, thus the following constraints are added to the design

$$W_1 = W_2,\ L_1 = L_2,\ W_5 = W_6,\ L_5 = L_6\ , \tag{6}$$

W_2 is selected to satisfy the desired polarization for this amplification stage. On the other hand, for the transistors M_7 and M_8 of the second amplification stage, the condition

$$\frac{W_8/L_8}{W_6/L_6} = 2\frac{W_7/L_7}{W_2/L_2} \tag{7}$$

must be satisfied in order to avoid an offset voltage at the output of the op-amp. Size of transistors are within a certain valid range of values depending on technology specifications; the width of transistors W_l are the independent parameters. In our case, therefore, they move between a minimum (W_{min}) and a maximum (W_{max}) value, as expressed in the next constraints:

$$W_{\min} \leq W_l \leq W_{\max}, \quad l = 1, 2, \cdots, 8 \tag{8}$$

while the largenesses of transistors L_i are fixed to a convenient value. The value of the compensation resistance (see [12]) is determined by:

$$R_c = \frac{1}{g_{m4}} \tag{9}$$

3. A Fuzzy System for the Op-Amp Design

A closed-loop Mamdani system is applied to reach a desired UGB with restrictions in OLG and PM. In this system, control actions are taken according to the experience in the op-amp; thus, the compensation capacitor C_c modifies UGB while W_3 and W_8 have influence over OLG and PM. Let us notice that W_4 and W_7 are tied to W_3 and W_8 respectively.

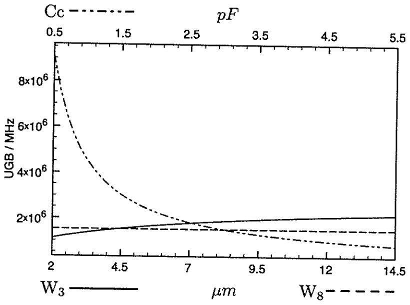
Figure 2 describes the behavior of UGB in MHz, OLG in dB and PM in degrees. This is obtained moving C_c from 0.5 to 5.5 pF, and both W_3 and W_8 from 2 to 14.5 μm. Figure 2(a) shows as well that the variation of W_8 does not affect UGB; meanwhile W_3 increments it in a gradual way. On the other hand, small increments of C_c produce a faster decrement of UGB.

Figure 2(b) shows that the variation of C_c does not change OLG, but W_3 and W_8 produce an increment of this value as they are increased. Thus, if it is desired an increment or decrement of OLG, we can use W_3 or W_8. Finally, C_c and W_8 have a direct impact over PM and W_3 has an inverse relationship, as it is described in Fig. 2(c).

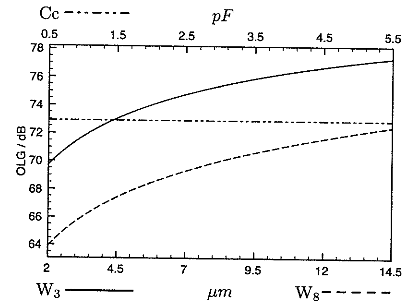
In order to determine the satisfiability, i.e. the membership degree for the design objective and restrictions, it is taken the relative error associated with each of them. It is important to point out that the sign of every relative error is useful to determine an increment or decrement in the associated variable. The fuzzy system is formed by three parts: input errors; inference system and control actions.

3.1 Input Errors

Each relative error has a different input fuzzy system, which is described in Fig. 3. For a fuzzification of the relative error associated with UGB (expresses as ϵ_{UGB}), we are making use of three fuzzy sets as shown in Fig. 3(a). Z set is employed to know if the input has reached the UGB objective, and N and P are employed to determine if the input value is above or below the desired UGB value respectively. Similarly, Fig. 3(b) shows two sets to fuzzify ϵ_{OLG}; in this case there is no need of a fuzzy set for an equality. PM is allowed to be in a range of values, therefore trapezoidal fuzzy sets are enough for a fuzzication of ϵ_{PM}; see Fig. 3(c).



(a)



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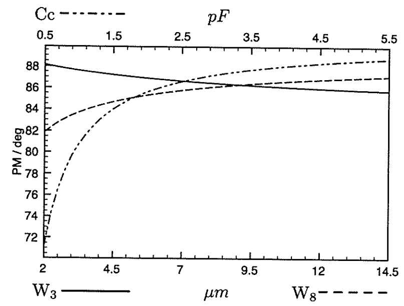


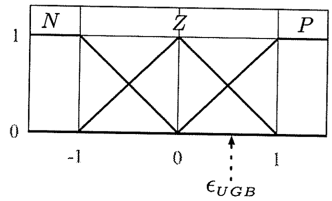
(c)

Fig. 2 Behavior of (a) UGB, (b) OLG and (c) PM.

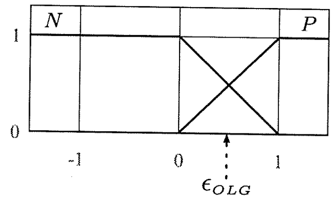
3.2 Inference System

The experience for the op-amp circuit is presented in Table 1, describing the relation between variables and design parameters. These relations in combination with the input fuzzy system (Fig. 3) give us 18 different cases with 9 possible control actions, which are expressed in a linguistic form. Table 2 presents the control actions for each one of the 18 cases, where Table 2(a) corresponds with a negative ϵ_{OLG} (so the OLG restriction is accomplished) and Table 2(b) agrees with a positive ϵ_{OLG}. In both tables, rows are associated with ϵ_{PM} and columns with ϵ_{UGBW}.

In the optimization process, the possible actions for the independent variables C_c, W_3 and W_8 are defined as follows: Increasing (Inc), No Action (NA) or Decreasing (Dec). On the other hand, each control action is crisped using the classical minimax criterion.



(a)



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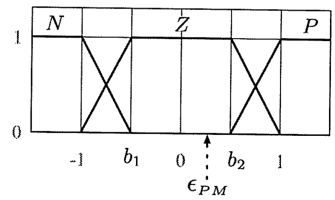

(c)

Fig. 3 Input fuzzy systems for computing the membership degrees: a) μ_f, b) μ_g and c) μ_h.

Table 1 Relations between independent variables and design parameters.

	Direct Proportion	Inverse Proportion	No Relation
UGBW	W_3	Cc	W_8
OLG	W_3, W_8		Cc
PM	Cc, W_8	W_3	

Table 2 Inference system for deciding the control actions of the fuzzy system.

(a) ϵ_{OLG} Negative

	ϵ_{UGB} Neg	ϵ_{UGB} Zero	ϵ_{UGB} Pos
ϵ_{PM} Neg	Dec W_3	Dec W_8	Dec Cc
ϵ_{PM} Zero	Dec W_3	NA	Dec Cc
ϵ_{PM} Pos	Dec W_3	Inc W_8	Dec Cc

(b) ϵ_{OLG} Positive

	ϵ_{UGB} Neg	ϵ_{UGB} Zero	ϵ_{UGB} Pos
ϵ_{PM} Neg	Inc Cc	Inc W_8	Inc W_3
ϵ_{PM} Zero	Inc Cc	Inc W_3	Inc W_3
ϵ_{PM} Pos	Inc Cc	Inc W_8	Inc W_3

3.3 Control Actions

Once the 9 control actions have been actualized with the minimax criterion, corrections to variables C_c, W_3 and W_8 are calculated. The correction process is the same for all variables; there is one membership degree for each control action that gives rise to the output fuzzy system (*see* Fig. 4), which is composed of three singleton sets. Thus, using the information from singletons and the centroid method, a crisp control action is obtained to update the related independent variable.

The fuzzy system here exposed has the advantage of being very simple and does not require a deep mathematical construction. However, one of its disadvantages is that the fuzzy sets for both input errors and output control actions, are statical during the optimization. It means that for small, but not negligible relative errors, there would be a slow convergence of the fuzzy system. In order to solve this inconvenience, the application of a neural network is proposed in next section.

4. A Neuro Fuzzy System for the Op-Amp Design

In order to obtain a faster convergence in the op-amp design, a Kohonen neural network is employed, with a learning factor (α) associated with every value defining a limit in both the input and output of the fuzzy systems. Therefore errors (input) and control actions (output) are now adaptive.

In the input, each error is compared with the value stored by its correspondent neuron; the *winner* neuron, i.e. the one with the minimum distance γ with regard to the relative error, moves the value towards the relative error according to a learning factor. This change in the winner neuron adjusts the universe of discourse of the fuzzy system, producing a major membership degree for obtaining a stronger control action and a faster convergence. When the winner neuron corresponds to the value zero, in all cases the input error is considered negligible, then the neuron is not changed ($\alpha = 0$). This process for the UGB is illustrated in Fig. 5.

Similarly, three Kohonen neurons, now with learning factor β, are associated to each output of the fuzzy system. The stored values in these neurons define the position of the singleton sets in the universe of discourse. Once calculated the value of a control action δ, it is compared with the values stored in the neurons; the winner neuron changes its value adjusting as well the output universe of discourse. This process generates an adaptive amplification of the control actions. Again, when the winner neuron is that with value zero, it is not change ($\beta = 0$). For the UGB, the output fuzzy system is shown in Fig. 6.

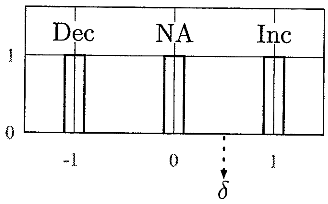

Fig. 4 Output fuzzy system for actualizing Cc, W_3 y W_8.

5. Implementation and Results

To test our proposed method we have implemented a program in C language using level 3 SPICE model for MOS transistors [13], with data files taken from a commercial 1.5 μm process. A length of 1.6 μm has been chosen for every transistor, so $L_1 = L_2 = \cdots = L_8 = 1.6\,\mu$m; and a width from 4.0 to 100 μm has been permitted for transistors $M_3, M_4, \cdots, M_8$. For transistors M_1 and M_2, a fix value $W_1 = W_2 = 24.0\,\mu$m has been applied. The power supply

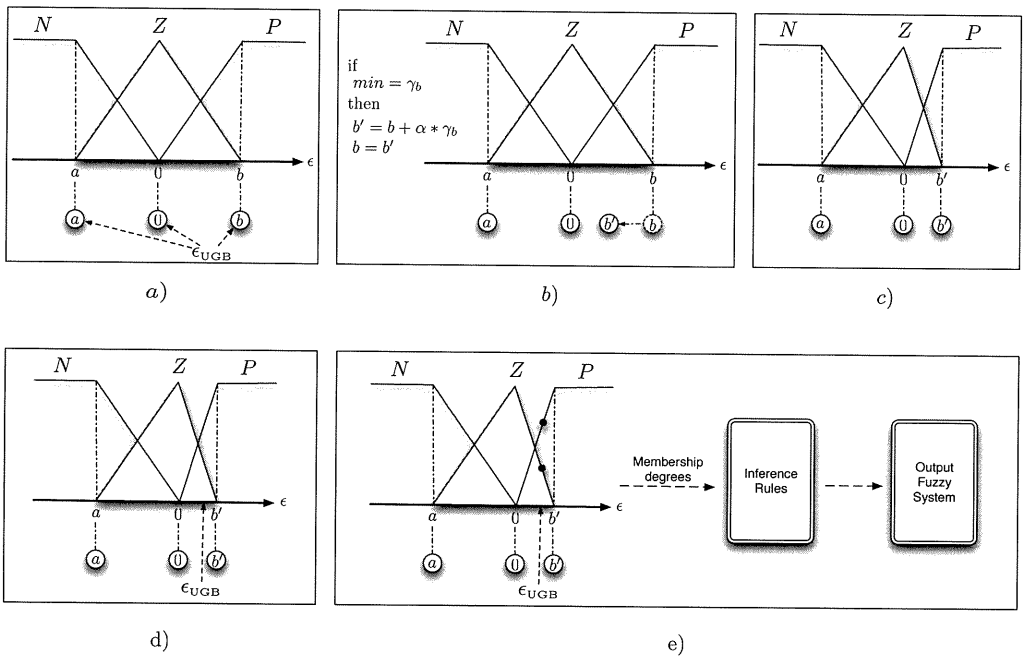

Fig. 5 Neuro fuzzy input system for UGB.

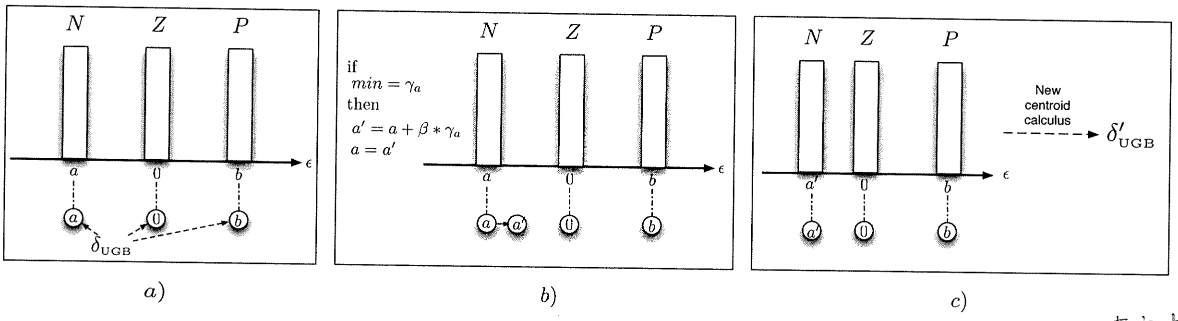

Fig. 6 Neuro fuzzy output system for UGB.

Table 3 Performances for the fuzzy system.

Iteration	Parameters			Performances			μ_f
	Cc (pF)	W_3 (μm)	W_8 (μm)	UGB (Hz)	OLG (dB)	PM (°)	
1	2.25	5.0	8.0	1921382	70.1	84.9	0.568
10	0.76	7.9	8.0	9885168	72.5	63.1	0.753
20	0.86	9.8	8.0	10057937	73.5	62.6	0.841
30	0.92	11.0	8.0	10039352	74.0	62.6	0.895
40	0.95	11.8	8.0	10026709	74.4	62.6	0.929
50	0.97	12.4	8.0	10018321	74.6	62.6	0.951
60	0.99	12.8	8.0	10012651	74.7	62.6	0.966
70	1.00	13.0	8.0	10008774	74.8	62.6	0.977
80	1.01	13.2	8.0	10006103	74.9	62.6	0.984
90	1.01	13.3	8.0	10004254	74.9	62.6	0.989
100	1.02	13.4	8.0	10002969	74.9	62.6	0.992
110	1.02	13.5	8.0	10002074	75.0	62.6	0.994
115	1.02	13.5	8.0	10001734	75.0	62.6	0.995

Table 4 Performances for the neuro fuzzy system.

Iteration	Parameters			Performances			μ_f
	Cc (pF)	W_3 (μm)	W_8 (μm)	UGB (Hz)	OLG (dB)	PM (°)	
1	2.06	5.3	8.0	1921382	70.1	84.9	0.568
5	0.56	7.4	8.2	8410238	72.2	67.1	0.724
10	0.87	8.6	8.4	11633440	73.1	59.5	0.808
15	0.84	9.9	8.4	9839025	73.7	63.7	0.861
20	0.91	10.8	8.4	10073234	74.1	63.1	0.905
25	0.94	11.5	8.4	10044415	74.4	63.1	0.935
30	0.96	11.9	8.4	10030884	74.6	63.1	0.955
35	0.97	12.3	8.4	10021576	74.7	63.2	0.969
40	0.98	12.5	8.4	10015125	74.8	63.2	0.978
45	0.99	12.6	8.4	10010627	74.9	63.2	0.985
50	0.99	12.7	8.4	10007479	74.9	63.2	0.989
55	0.99	12.8	8.4	10005269	74.9	63.2	0.992
60	1.00	12.9	8.4	10003715	75.0	63.2	0.995

is $V_{DD} = -V_{SS} = 5$V while the value of bias current (I_{Bias}) is 25 μA. Finally, a load capacitance C_L of 1.0 pF has been assumed.

The design objective for the op-amp is to achieve a UBW equal to 10 MHz, with at least 75 dB of OPG; the PM is required to be in the range of 60° and 90°. The design will be considered finished when a grade of satisfiability of 99.5% is reached for each membership function. Table 3 and Table 4 shows parameters and performances evolving for the fuzzy and neuro fuzzy design respectively. Both tables also shows μ_f, the most demanding grade of satisfiability. As

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Table 5 Design results for the op-amp.

Transistor channel sizes:	$W_1 = W_2 = 24.0\,\mu$m $W_3 = W_4 = 12.9\,\mu$m $W_5 = W_6 = 4.2\,\mu$m $W_7 = 24.0\,\mu$m $W_8 = 8.4\,\mu$m $L_1 = L_2 = 1.6\,\mu$m $L_3 = L_4 = 1.6\,\mu$m $L_5 = L_6 = 1.6\,\mu$m $L_7 = 1.6\,\mu$m $L_8 = 1.6\,\mu$m
Compensation components:	Cc = 1.00 pF Rc = 2415 Ω

Please refer to Table 5 in your text.

Table 6 Performance of the optimized op-amp.

	Program	HSPICE
Open-loop gain : (dB) Required: (≥ 75 dB)	75.0	78.3
Unity-gain bandwidth: (MHz) Required: (= 10 MHz)	10.0	9.5
Phase margin: (deg) Required: (60° ≤ PM ≤ 90°)	63.2	58.0

can be seen, the number of iterations needed to optimize an op-amp diminish drastically with the use of a neuro fuzzy system rather than a fuzzy system along, 115 against 60 iterations respectively which means an improvement of 48%. This fact shows that the use of a simplified neural network of Kohonen type is useful to adjust the universe of discourse of a fuzzy system obtaining a faster design process.

The performance of the optimized op-pamp is shown in Table 6, where Program column shows data obtained with our implementation that is validated with the column corresponding to HSPICE simulation using level 3 models for NMOS and PMOS transistors. The UGB, 10.0 MHz, of the op-amp that was designed with our Program is very close to the value obtained with HSPICE software, 9.5 MHz. There is a slight difference in PM, 63.2° that we obtained compared with 58.0° obtained with HSPICE. On the contrary we see a difference of 3.3 dB on OLG between our approach and the specialized software. Thus, this validation may be considered as satisfactory, taken into account the differences between transistor models in each case.

6. Conclusions

In this paper we have presented a fuzzy method to design analog circuits. A neural network of Kohonen type has been implemented to improve the control of the universe of discourse in the fuzzy system. Design objectives for an op-amp circuit have been fulfilled using the proposed methodology, and a validation with a robust commercial software has been successful. Further work may imply an improvement in transistor models; and the automatization of the inference system deduction in order to reduce the complete design time.

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